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L13	58	L11 and simulat\$5.ti.	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2005/10/31 15:44
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IEEE JNL IEEE Journal or Magazine

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IEEE STD IEEE Standard

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- ☐ **1. A 2.5 Gb/s ATM switch chip set**
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- ☐ **2. Design of embedded systems: formal models, validation, and synthesis**
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- ☐ **3. Core design and system-on-a-chip integration**
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- ☐ **4. Scalable hardware priority queue architectures for high-speed packet swi**
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- ☐ **5. Design and modelling of a high performance differential bipolar self-time microprocessor**
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- ☐ **9. High-density zero suppressor and encoder VME board using field program array**
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» Key

IEEE JNL IEEE Journal or Magazine

IEE JNL IEE Journal or Magazine

IEEE CNF IEEE Conference Proceeding

IEE CNF IEE Conference Proceeding

IEEE STD IEEE Standard

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